

**REMARKS**

Claims 1-13 are presented for examination.

FIG. 2 of the drawings has been amended to correct typographical errors in blocks 18, 40, 42 and 44 and to make the drawings consistent with the specification.

**REJECTION UNDER 35 U.S.C. 102**

Claims 1-3 have been rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka.

**Rejection of claim 1**

Claim 1 has been amended to more clearly define the claimed invention over the reference. Claim 1, as amended, recites, among other features, a scrambling circuit for converting a plurality of input signals respectively representing test results for a plurality of elements to a desired format. The claim requires the scrambling circuit to include a plurality of conversion circuits for respectively converting said plurality of input signals according to different rules. Tanaka does not disclose this arrangement.

The Examiner considers Tanaka's byte swap circuit 13 and word swap circuit 14 to correspond to the conversion circuits. The byte swap circuit 13 converts two-byte data elements provided by the input circuit 11. The word swap circuit 14 converts first data inputted by the input circuit 11. Therefore, they do not convert signals representing test results for a plurality of elements.

It is noted that the Examiner applies a combination of Tanaka with Tabata et al. to reject the subject matter of claim 13 that recites testing a semiconductor device. It is submitted that the combination of Tanaka with Tabata et al. does not teach or suggest the structure recited in claim 1. In particular, neither Tanaka nor Tabata et al. suggests converting plurality of input signals, respectively representing test results for a plurality of elements, according to different rules. Therefore, this combination is not sufficient to suggest the claimed arrangement.

Accordingly, claim 1, as amended, is defined over the applied references.

**Rejection of claims 2 and 3.**

The Examiner's rejection with respect to claims 2 and 3 is respectfully traversed for the following reasons.

Independent claim 2 recites among other features a scrambling circuit for converting an input signal to a desired format. The claim requires the scrambling circuit to be constituted by a rewritable device.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied*, 110 S.Ct. 154 (1989).

The Examiner considers the data transfer device 1 in FIG. 2 of Tanaka to correspond to the claimed scrambling circuit, and relies upon col. 1, lines 5-11 for teaching that the scrambling circuit is constituted by a rewritable device.

Considering the reference, Tanaka discloses a data transfer device for transferring data between memories or between a memory and a data processing device. The reference specifies that the data transfer device converts byte order of data blocks formed from data elements of different lengths, and transfers the converted data blocks (col. 1, lines 5-11).

Accordingly, the reference does not expressly disclose that the data transfer device 1 is constituted by a rewritable device.

To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability

or possibilities. *In re Robertson*, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

Applicants respectfully assert that the record fails to meet this requirement.

Moreover, as shown in FIG. 2, the data transfer device 1 arranged between two system buses comprises a control circuit, two address counters, and multiple data processing and input/output elements. It is submitted that one skilled in the art would recognize that the data transfer device 1 shown in FIG. 2 is not constituted by a rewritable device, as claim 2 requires.

Claim 3 dependent from claim 3 is defined over the reference at least for the reasons presented above in connection with claim 2.

Applicants, therefore, respectfully submit that the rejection of claims 2 and 3 under 35 U.S.C. § 102 as anticipated by Tanaka is untenable and should be withdrawn.

REJECTIONS UNDER 35 U.S.C. 103

Claims 4-12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka. This rejection is respectfully traversed for the following reasons.

First, claims 4-12 depend from either claim 1 or claim 2. Therefore, they are defined over Tanaka at least for the reasons presented above in connection with claims 1 and 2.

Moreover, the Examiner admits that Tanaka does not disclose the subject matter of claims 4-12. However, he takes the Official Notice that the subject matter of these claims is well known.

The Examiner's position is respectfully traversed. It is respectfully submitted that the prior art does not teach or suggest the scrambling circuit arranged in the manner required by claims 4-12. As the Examiner relies upon "well known" prior art, he is respectfully requested to cite a reference in support of his position (see MPEP 2144.03).

Claim 13 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Tabata et al. This rejection is respectfully traversed for the following reasons.

First, claim 13 depends from claim 1. Therefore, it is defined over the prior art at least for the reasons presented above in connection with claims 1.

Further, the Examiner admits that Tanaka does not disclose the tester for supplying the scrambling circuit with results of the testing. Tabata et al. is relied upon for disclosing this feature.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to provide a basis in fact and/or cogent technical reasoning to support the conclusion that one having ordinary skill in the art would have been motivated to combine references to arrive at a claimed invention.

*Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988). The Examiner offered no logical reason, and no such reason is apparent, to support the conclusion that one having ordinary skill in the art would have been impelled to combine Tanaka and Tabata et al.

Considering the references, Tanaka discloses a data transfer device that receives data elements of different lengths in each data block provided by a transfer source. The data transfer device converts these data elements into an endian format.

Tabata et al. discloses a memory tester that supplies a failure analysis memory with test results. The failure analysis memory is supplied with address data AD and failed data FD. Neither address data AD nor failed data FD are composed of data elements having different lengths in each data block. Moreover, the reference does not disclose that the failed analysis memory stores data in an endian format.

Accordingly, one skilled in the art would have no reason to use the tester of Tabata et al. for supplying the data transfer device of Tanaka. Hence, the Examiner's conclusion of obviousness is not warranted.

Applicants, therefore, respectfully submit that the rejections of claims 4-13 under 35 U.S.C. § 103 are improper and should be withdrawn.

In view of the foregoing, and in summary, claims 1-13 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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